#6 7/8/03 VE

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Patent

Attorney Docket No. MTI-31267

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant (s)	:	Polinsky et al.
Serial No.	:	~~09/584,975~~ 09/854975
For	:	Modified Facet Etch to Prevent Blown Gate Oxide and Increase Chamber Life
Filed	:	May 14, 2001
Examiner	:	Lynette T. Umez Eronini
Group Art Unit	:	1765
Confirmation No.	:	0989

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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Date: July 7, 2003

Rosa Stong

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE AFTER FINAL REJECTION UNDER 37 C.F.R. § 1.116

This response replies to the Final Office Action mailed May 6, 2003 (Paper No. 5).

The Applicant repeats all of the previously submitted arguments below. First, though, the Applicant wishes to comment on the Examiner's Response to Arguments.

Regarding the §112 rejections, the Applicant argued that the terms "predetermined depth" and "target depth" were both standard terms in the art and supported this argument with examples of issued U.S. patents which used these terms in similar fashion as the currently pending claims. The Applicant wishes to emphasize this support by noting for the Examiner's attention that over 3600 U.S. patents use one or the other of these terms in their claims. See

attached cover sheet of a search result on the USPTO database. Although, the Applicant has not reviewed all of these U.S. patents, a random sampling indicates that the Applicant has used standard terms in their standard usage. See, e.g., USP 6,586,702 and 6,583,054 claims attached. In response to the Applicants well-supported arguments that both "predetermined depth" and "target depth" are standard terms in the art the Examiner raises two points: (1) that the terms fail to define over a generic depth and (2) that claim 9 of USP 6,511,777 defines the predetermined depth specifically. The Applicant believes that both of the Examiner's points are in error.

There are at least two reasons why the Examiner's first point is in error. First, as argued above, the terms in dispute are standard terms of art which must relate to a specific depth that is understood by one skilled in the art. As such, the use of these terms to identify a certain depth must, by definition, be different than a generic depth or else the at least 3600 persons skilled in the art (as represented by the issued U.S. patents) would not have used the terms. Second, the Examiner is completely discounting the ability of those skilled in this art. Such a skilled person would not be etching the substrate unless the design and production process of the semiconductor chip requires such etching. Such design and process considerations would also include the target depth to which the etch is conducted. In other words, one skilled in the art would not begin an etching process unless that person knew when to terminate the etch. Determination of the target depth is not the subject of the current claims, but rather, the subject is a method facet etching to a predetermined depth. As such, one skilled in the art would recognize that determining the absolute magnitude of the predetermined target depth was merely a design consideration of the chip being manufactured and not part of the current invention. Therefore, the specification, e.g., page 5, line 21 through page 6, line 4, FIG. 4 and FIG. 5, fully enables and supports the terminology of the current claims.

The Examiner's second point is also clearly in conflict with U.S. patent laws. Specifically, claim 9 of the US'777 patent that the Examiner cites is merely a dependent claim that further defines and limits the term "predetermined depth". Apparently, the Examiner is either reading the limitations of dependent claim 9 into the claims it depends from (all of which use the term "predetermined depth" without further description) or is assuming that those preceding claims are all invalid. As the Examiner is aware, all claims of a U.S. patent are

presumed to be valid. Additionally, the Examiner is surely aware that limitations from dependent claims are not to be read into the independent claims. As such, even in the patent that the Examiner cites, the term "predetermined depth" is used in at least Claims 1-8, without additional description. Moreover, the Examiner's contention, even if it were correct (which the Applicant denies), only addresses one patent, not the entire list of support that the Applicant cites.

Regarding the §103 rejections, the Examiner has failed to address the Applicant's contentions that the Examiner's proposed combination of references is legally barred. Specifically, the Examiner has not responded to the arguments that Yao teaches away from the current invention because the unexpected results reported by Yao are stated to be due to the specific sequential steps. Likewise, the Examiner has not responded to the argument that the combination with Yao is legally barred because such a combination would change the principle of operation of Yao.

Accordingly, the Applicant believes that the following previously submitted arguments, when viewed in conjunction with the above remarks, persuasively traverse all of the Examiner's rejections.

The Examiner finally rejected Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner finds the meaning of the term "target depth" unclear. Additionally, the Examiner finds the term "predetermined" indefinite because it reads on a nebulous metal step conducted prior to manipulative steps of the claimed invention. The Applicant traverses these rejections as follows.

The term "target depth" is clear from the claims, is fully described in the specification and is a standard term of art. The claims clearly state that target depth is the depth at which the inventive etching process is terminated. See preamble to Claim 1 and final step of each independent claim. Additionally, the term is used unambiguously to mean such throughout the specification. Moreover, the term "target depth" is a term of art found in the granted claims of other U.S. patents which, are of course, presumed to be valid with respect to all sections of the

statute. As an example, attached are the Claims pages from USP 6,225,234 obtained off the USPTO database. The Examiner will note in Claim 1 the use of the term "target depth" in a manner identical to the manner of the current claims. As such, the Examiner's rejection is in error and should be withdrawn.

Likewise, the term "predetermined depth" is a standard term found in numerous U.S. patents. As examples, attached are the Claims pages for USP Nos. 6,518,624 and 6,511,777 which demonstrate the use of the term "predetermined depth" in a manner identical to the current claims. As such, the Examiner should reconsider and withdraw his rejections based on § 112, paragraph 1.

The Examiner finally rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Doan (USP 5,346,585) in view of Laxman (USP 5,774,196) in view of Yao et al. (USP 5,814,564). The Examiner states that Doan teaches a method for facet etching a semiconductor device to a target depth. The Examiner admits that Doan fails to teach both that the first layer is formed to a thickness at least equal to the target depth and that the specified depth in which the first etch is terminated with respect to the target depth. The Examiner then relies on Laxman to demonstrate that the layer thickness is a results effective variable. The Examiner then also admits that Doan in view of Laxman fails to teach: terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth; etching the first layer in a second etch by contacting the first layer with a reactive chemical gas/plasma; and terminating the second etch when the first layer has been etched to the target depth. The Examiner then relies on Yao et al. for the teaching of a method of etching back an oxide layer by employing six etching steps. The Examiner states that "since each of these steps are performed in a specified time, then using Yao et al.'s steps of etching an oxide layer would inherently read on [the current claims]". The Applicants traverse on the grounds that the cited prior art fails to teach all elements of the invention and are not properly combinable.

Specifically, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP §2143.03 (citing to *In re Royka*, 180 USPQ 580 (CCPA 1974)). Moreover, showing that the prior art can be combined or modified is not sufficient, of itself, to establish *prima facie* obviousness. See MPEP §2143.01.

Nor can an obviousness rejection be supported merely by showing that it would be "obvious to try" the claimed invention. See, e.g., *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Rather, in order to establish a *prima facie* case of obviousness, the Examiner must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. Furthermore, in leading one skilled in the art, the prior art must suggest to the ordinary skilled artisan that the combination should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. *In re Dow Chemical Co*, 5 USPQ2d 1529, 1532 (Fed. Cir. 1988)(emphasis added). Indeed, both the suggestion and the expectation of success must be found in the prior art, not in the Applicant's disclosure. Id. More specifically, the Federal District Court of D.C., which has jurisdiction over the USPTO, recently ruled that the suggestion or motivation to modify or combine prior art must be explicit in the prior art. See *Winner Int'l. Royalty Corp. v. Wang*, 48 USPQ2d 1139 (DCDC 1998). Moreover, a prior art reference must be considered in its entirety with consideration given to disclosures that diverge or teach away from the invention at issue as well as disclosures which direct the skilled artisan to the invention. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 300 (Fed. Cir. 1985). The Applicants believe that the Examiner's § 103 rejections fail to meet the above standards.

First, as the Examiner has stated, Doan teaches facet etching a semiconductor device to a target depth. Thus, Doan does not teach terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth. There is no disclosure or suggestion in Doan of terminating the etch prior to the target depth or using a two-stage etch. Indeed, for the purposes of Doan, terminating the facet edge prior to reaching the target depth would be unsuitable because the target depth would not then be reached. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Moreover, a two stage etch, wherein the second stage etch is done by contacting the first layer with a reactive chemical gas/plasma, is a different principle of operation from a one stage etch performed exclusively with a plasma beam as taught in Doan. As such, Doan fails to teach or suggest the current invention and may not be properly modified as proposed by the Examiner.

The Examiner's use of Laxman does not advance the proposed *prima facie* case. Indeed, the teaching of Laxman is irrelevant to the current invention. The teaching of Laxman, at best, may be interpreted to indicate that layer thickness is a result effective variable in some context but the teaching does not indicate that layer thickness is a result effective variable in the context of the current method of facet etching. While the thickness of an insulating layer may well affect the performance of a semiconductor device, the layer thickness does not affect the performance of the current method. In other words, one skilled in the art would not change the thickness of a layer expecting to improve or alter the performance of the current method. Rather, the operational parameters of the current method would be optimized for different layer thicknesses. Moreover, even if Laxman did render the thickness of the first layer obvious (which the Applicant strongly denies) it adds no teaching whatsoever regarding the relationship between the thickness of the first layer and the target depth.

The combination of Yao et al. and the combined teachings of Doan and Laxman is neither proper nor provides the missing teachings. The Examiner states that the sixth step etch of Yao et al. inherently covers the current claims. However, the Applicants believe that the Examiner has failed to meet the stringent requirements of an obviousness rejection based upon inherency.

In order to establish a *prima facie* case of obviousness based on inherent properties, the Examiner must show that the undisclosed properties are not only inevitably and necessarily present, but also that the inherency of the undisclosed properties or elements is obvious to one skilled in the art. *Kloster Speedsteel AB v. Crucible Inc.*, 230 USPQ 81, 88 (Fed. Cir. 1986).

There is no teaching or suggestion in Yao et al. which would obviously indicate to one skilled in the art that the two step etch of the current claims is necessarily and inevitably the result of the teaching of Yao et al.

Moreover, not only does Yao et al. not inherently cover the current claims, Yao et al. explicitly teaches away from the methods of the current claims. Yao et al. state that their unexpected results are due to the specific combination of steps 2-5. See column 3, lines 1-10. However, the sequential steps of Yao et al. are in reverse order to the steps of the current method.

In other words, Yao et al. teaches away from the claimed sequence of steps. The Applicants also point to the following differences between Yao et al. and the current claims.

Furthermore, Yao et al. performs chemical etching prior to plasma etching. This is a different principle of operation than the current claims. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Moreover, the goal of Yao et al. is to obtain a highly smooth planarized surface. Modifying the teachings of Yao et al. to do a facet etch would render the surface distinctly non-planar and as such, would be unusable for the purpose of Yao et al. In addition, Steps 3-6 of Yao et al. etches the semiconductor device beyond the first layer. This means that the target depth of the etch of Yao et al. is greater than the depth of the first layer contrary to the language of the current claims. For the above reasons, even if, arguendo, Yao et al. were properly combinable with Doan in view of Laxman, such a combination fails to teach the steps of the current method claim. Therefore, the Examiner should reconsider and withdraw the rejections of Claims 1-10 under § 103(a).

The Examiner finally rejected Claims 11-21 under 35 U.S.C. § 103(a) as being unpatentable over Doan in view of Laxman and Yao et al. and further in view of Lee (USP 5,935,875). The Applicants respectfully traverse this rejection. As argued above, the combination of Doan in view of Laxman in view of Yao et al. is not proper and also fails to disclose the elements of the current claims. The above arguments are repeated herein by reference. The addition of Lee does not remedy the deficiencies in the combined teachings of Doan in view of Laxman and Yao et al. nor does it render such a combination proper. As such, this rejection is improper and the *prima facie* case fails.

No fee is believed due for the filing of this response. If a fee is due, such fee should be charged to Deposit Account 23-2053 and any necessary petition should be considered provisionally made.

Respectfully submitted,

Dated: July 7, 2003

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Searching 1976 to present...

Results of Search in 1976 to present db for:
ACLM/"predetermined depth" OR ACLM/"target depth": 3639 patents.
Hits 1 through 50 out of 3639

Next 50 Hits

Jump To

Refine Search ACLM/"predetermined depth" OR ACLM/"target depth"

	PAT. NO.	Title
1	6,586,702	High density pixel array and laser micro-milling method for fabricating array
2	6,584,751	High speed machine for inserting sheets into envelopes
3	6,583,381	Apparatus for fabrication of miniature structures
4	6,583,054	Method for forming conductive line in semiconductor device
5	6,583,032	Method for manufacturing semiconductor chips
6	6,582,445	Trephine for lamellar keratectomy
7	6,579,282	Device and method for creating a corneal reference for an eyetracker
8	6,578,321	Embeddable mounting device
9	6,577,051	Flat cathode ray tube
10	6,576,407	Method of improving astigmatism of a photoresist layer
11	6,575,882	Exercise device having weights and safety mechanism to maintain weights in place
12	6,575,712	Air compressor system
13	6,575,436	Evaporative cooler
14	6,575,313	Structure for firmly resting tools thereon
15	6,575,192	Check valve for a prechamber assembly
16	6,574,984	Refrigerator door mounted water dispensing assembly
17	6,574,494	Methods, systems and computer program products for photogrammetric sensor position estimation
18	6,574,433	Underwater camera housing
19	6,573,583	Semiconductor device and method of manufacturing the same
20	6,573,136	Isolating a vertical gate contact structure

United States Patent **6,583,054**
Kwon **June 24, 2003**

Method for forming conductive line in semiconductor device

Abstract

Provided with a method for forming conductive lines in a semiconductor device including the steps of: (a) forming a first conductive line on a substrate; (b) forming a first insulating layer on the substrate as well as on the first conductive line; (c) etching the first insulating layer on the first conductive line to form a first opening; (d) forming a second insulating layer on the first insulating layer to be in contact with the upper part of the first opening, thereby sealing the first opening; (e) etching the first and second insulating layers corresponding to the first conductive line to form a second opening and at the same time extend the first opening so as to expose the first conductive line; and (f) forming a second conductive line within the first and second openings so as to be connected with the first conductive line, thereby preventing halation caused by irregular reflection during exposure on the second photo resist because the second insulating layer has a less difference in thickness, and suppressing decrease in the exposed area of the first conductive line caused by extension of the first opening.

Inventors: **Kwon; Tae-Seok** (Chungcheongbuk-do, KR)
Assignee: **Hyundai Microelectronics Co., Ltd.** (Chungcheongbuk-do, KR)
Appl. No.: **421092**
Filed: **October 19, 1999**

Forcign Application Priority Data

Feb 22, 1999[KR] 1999-5794

Current U.S. Class: **438/638**; 438/624; 438/627; 438/706; 438/786
Intern'l Class: H01L 021/476.3; H01L 021/302; H01L 021/469
Field of Search: 438/622-624,627,629,631,633,637-640,700,706,786,791

References Cited [Referenced By]

U.S. Patent Documents

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6228758	May., 2001	Pellerin et al.	

Primary Examiner: Nguyen; Ha Tran
Attorney, Agent or Firm: Morgan, Lewis & Bockius LLP

Claims

What is claimed is:

1. A method for forming conductive lines in a semiconductor device comprising the steps of:

(a) forming a first conductive line on a substrate;

(b) forming a first single insulating layer on the substrate as well as on the first conductive line;

(c) etching the first single insulating layer on the first conductive line to form a first opening;

(d) forming a second insulating layer on the first single insulating layer to be in contact with the upper part of the first opening, thereby sealing the first opening and defining a void at a lower part of the first opening;

(e) etching the first single and second insulating layers corresponding to the first conductive line to form a second opening and at the same time extend the first opening so as to expose the first conductive line; and

(f) forming a second conductive line within the first and second openings so as to be connected with the first conductive line.

2. The method as claimed in claim 1, wherein the step (c) of forming the first opening comprises the steps of:

forming a first photo resist on the first single insulating layer to expose a portion corresponding to a portion of the first conductive line; and

etching the first single insulating layer as deep as a ***predetermined depth*** by using the first photo resist as a mask.

3. The method as claimed in claim 1, wherein the second insulating layer is deposited to have overhangs occurring at the upper edge of the first opening and being in contact with one another to seal the first opening.

4. The method as claimed in claim 3, wherein the second insulating layer is formed by a plasma enhanced chemical vapor deposition using SiH.sub.4 or TEOS (tetraethyl orthosilicate) as a reactive gas, or by a sputtering method.

5. The method as claimed in claim 1, wherein the step (e) of forming the second opening comprises the steps of:

forming a second photo resist on the second insulating layer so as to expose a portion including a portion corresponding to the first opening; and

etching the first single and second insulating layers by using the second photo resist as a mask.

6. The method as claimed in claim 5, wherein the second opening is wider than the first opening.

7. The method as claimed in claim 1, wherein the step (f) of forming the second conductive line comprises the steps of:

depositing the second conductive line on the second insulating layer to fill the first and second openings; and

performing an etch back upon the second conductive line so as to expose the second insulating layer.

8. The method as claimed in claim 7, further comprising the steps of removing the second insulating layer.

9. The method as claimed in claim 1, further comprising the steps of forming a barrier metal layer on the surface of the first and second openings.

10. The method as claimed in claim 9, wherein the barrier metal layer is formed by continuously depositing titanium (Ti) and titanium nitride (TiN) by a sputtering method.

11. The method as claimed in claim 9, wherein the step (f) of forming the second conductive line comprises the steps of:

depositing a conductive material on the barrier metal layer to fill the first and second openings; and

performing an etch back upon the conductive material and the barrier metal layer so as to expose the second insulating layer.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for fabricating a semiconductor device and, more particularly, to a method for forming conductive lines in a semiconductor device in which a trench for forming the upper conductive line is overlapped with contact holes for exposing the lower conductive line, the trench being filled with a conductive metal to form the upper conductive line.

United States Patent **6,586,702**
Wiener-Avnear , et al. **July 1, 2003**

High density pixel array and laser micro-milling method for fabricating array

Abstract

A pixel array device is fabricated by a laser micro-milling method under strict process control conditions. The device has an array of pixels bonded together with an adhesive filling the grooves between adjacent pixels. The array is fabricated by moving a substrate relative to a laser beam of predetermined intensity at a controlled, constant velocity along a predetermined path defining a set of grooves between adjacent pixels so that a predetermined laser flux per unit area is applied to the material, and repeating the movement for a plurality of passes of the laser beam until the grooves are ablated to a desired depth. The substrate is of an ultrasonic transducer material in one example for fabrication of a 2D ultrasonic phase array transducer. A substrate of phosphor material is used to fabricate an X-ray focal plane array detector.

Inventors: **Wiener-Avnear; Eliezer** (Carlsbad, CA); **McFall; James Earl** (Carlsbad, CA)
Assignee: **Laser Electro Optic Application Technology Company** (Carlsbad, CA)
Appl. No.: **780059**
Filed: **February 9, 2001**

Current U.S. Class: **219/121.6**; 219/121.69; 219/121.72
Intern'l Class: B23K 026/00
Field of Search: 219/121.6,121.67,121.68,121.69,121.72 428/209,195

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Primary Examiner: Elve; M. Alexandra
Attorney, Agent or Firm: Brown Martin Haller & McClain, LLP

Goverment Interests

The U.S. Government has rights in this invention pursuant to contract DAMD17-96-C-6032 awarded by the U.S. Department of Defense and contracts NAS9-00008 and NAS9-00119 awarded by NASA under the Small Business Innovation Research (SBIR) Program.

Parent Case Text

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation-In-Part of application Ser. No. 09/557,114 filed Apr. 24, 2000 which was a Continuation of application Scr. No. 09/275,537 filed on Mar. 24, 1999, now U.S. Pat. No. 6,087,618, which was a division of application Ser. No. 08,937,522, filed Sep. 25, 1997, now U.S. Pat. No. 5,956,382.

Claims

We claim:

1. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of a substrate material by application of a predetermined uniform flux per unit area; and

the relative movement of the substrate material and laser beam along each line in said set of lines being repeated until the material has been ablated sufficiently to form a groove of a ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels, each pixel having a first end at said first surface and a second end; and

covering the first ends of the pixels with a layer of acoustic matching material extending over the pixels, whereby the resultant pixel array can transmit and received ultrasonic waves.

2. The method as claimed in claim 1, including the step of adjusting the focus of the laser at periodic intervals after a predetermined number of passes of the laser beam along the groove.

3. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of piezoelectric transducer material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along each line in said set of lines being repeated until the material has been ablated sufficiently to form a groove a ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels; and

filling the grooves with glue material, the glue comprising a flexible epoxy material.

4. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric transducer material to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area; and

the relative movement of the substrate material and laser beam along each line in said set of lines being

repeated until the material has been ablated sufficiently to form a groove of ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels.

5. The method as claimed in claim 4, wherein the piezoelectric material is selected from the group consisting of relaxor ferroelectric materials, piezoelectric single crystals, and piezoelectric ceramics.

6. The method as claimed in claim 5, wherein the piezoelectric material is a relaxor ferroelectric material selected from the group consisting of PZN-PT and PMN-PT.

7. The method as claimed in claim 5, wherein the piezoelectric material is a piezoelectric single crystal selected from the group consisting of barium titanate and lithium tantalate.

8. The method as claimed in claim 5, wherein the piezoelectric material is a piezoelectric ceramic comprising a selected composition of lead zirconate titanate (PZT).

9. The method as claimed in claim 1, wherein the relative movement between the laser beam and substrate follows a path along each of the grooves, and then follows the same path repeatedly for a predetermined number of passes until the grooves are ablated to the ***predetermined depth***.

10. The method as claimed in claim 9, wherein the number of passes of the laser beam along each groove is in the range from 10 to 120.

11. The method as claimed in claim 10, wherein the focus of the laser beam is adjusted by 2 to 6 microns after each 10 passes of the laser beam.

12. The method as claimed in claim 1, wherein the laser beam has a Q-switched pulsed output, and the first pulse of the laser output is eliminated prior to application of the laser output to the substrate.

13. The method as claimed in claim 1, including the step of controlling operation of the laser beam in conjunction with the relative movement of the substrate and laser beam such that the laser beam is actuated only when the relative movement is at a constant velocity.

14. The method as claimed in claim 1, wherein the relative movement is a computer-controlled, constant velocity movement along a set of predetermined paths.

15. The method as claimed in claim 14, wherein at least some of the paths are linear.

16. The method as claimed in claim 14, wherein at least some of the paths are curved.

17. A method for micro-milling a substrate to a ***predetermined depth,*** comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate to be micro-milled;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along each line in said set of lines being

repeated until the material has been ablated sufficiently to form a groove of ***predetermined depth***;

whereby grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels; and

the grid pattern comprising a circular array, with a first set of the grooves being formed in spaced, concentric, circular paths of increasing diameter, and a second set of the grooves comprise a series of spaced lines extending transversely between each adjacent pair of circular grooves.

18. The method as claimed in claim 4, wherein the velocity is in the range from 25 .mu.m/sec to 24.times.10.sup.3 .mu.m/sec.

19. A method of forming an ultrasonic transducer for sending and receiving ultrasonic waves, comprising the steps of:

directing a laser beam at a predetermined intensity towards a first surface of a substrate of a piezoelectric material, the material having a second surface parallel to said first surface;

moving the substrate material relative to the laser beam at a predetermined constant velocity along a predetermined path so as to ablate a series of grooves in the surface of the substrate material by application of a predetermined uniform flux per unit area;

the relative movement of the substrate material and laser beam along said path being repeated for a predetermined number of passes until the material has been ablated sufficiently to form a groove of predetermined depth;

whereby the grooves are ablated in a predetermined grid pattern to form a series of pixels with kerfs or grooves separating the pixels, each pixel having a first end at said first surface and a second end at said second surface;

mounting an electrode at the second end of each pixel;

connecting the electrodes to transmitter and receiver electronics; and

encasing the second ends and electrodes in a layer of backing material.

20. The method as claimed in claim 19, including the step of covering the first ends of the pixels with a layer of acoustic matching material extending over the pixels.

Description

BACKGROUND OF THE INVENTION

The present invention is generally concerned with high density pixel array systems, such as imagers, sensors, actuators, detectors and the like, and methods of fabricating such arrays, and is particularly concerned with a method of fabricating a high performance pixel array in exotic materials such as ferroelectric, piezoelectric, pyroelectric, acousto-optic materials and the like for integration in such a system.